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## APPLICANTS

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 \*\* CONTINUING DATA \*\*\*\*\* *U/A*

 \*\* FOREIGN APPLICATIONS \*\*\*\*\* *Yes JP*  
 JAPAN 2002-354208 12/05/2002

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

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Verified and Acknowledged Examiner's Signature <i>[Signature]</i> Initials <i>JP</i>	JAPAN	10	12	3

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## TITLE

Design method of logic circuit

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